Notice of Allowability	Application No.	Applicant(s)	
	09/902,553	GFELLER ET AL.	
	Examiner	Art Unit	
	Krista M. Flanagan	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment from 05 May 2005*.

2. ☒ The allowed claim(s) is/are *1, 3-12, 14-17 and 19-26*.

3. ☒ The drawings filed on *10 July 2001* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20050809* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. The application has been amended as follows: Claim 19, "Method according to claim 18 further comprising..." has been amended to read -Method according to claim 17 further comprising...-

DETAILED ACTION

Specification

2. In view of the amendment filed on 05 May 2005, the Examiner withdraws objections to the specification from the previous Office Action.

Claim Objections

3. In view of the amendment filed on 05 May 2005, the Examiner withdraws objections to the claims from the previous Office Action.

Allowable Subject Matter

4. Claims 1, 3-12, 14-17, and 19-26 are allowed.

5. The following is an examiner's statement of reasons for allowance: The prior art does not show the bolded limitations in combination with the signal quality determination method and apparatus limitations.

a. Regarding claim 1, an apparatus for determining the quality of a digital signal, comprising a sampler using clock cycles for sampling the digital signal with a number n of samples per defined pulse width, whereby $n \geq 1$: an edge detector for detecting an edge of a pulse of the sampled digital signal; a counter for counting the clock cycles between edges detected by the edge detector; deviation detector being able to compare the counted clock cycles with a prestored reference-value in order to provide a deviation value as a measure for the instantaneous quality of

the digital signal; **and an absolute-value limiter unit for generating an absolute deviation value in response to the deviation value and a storage latch for storing the absolute deviation value.**

b. Regarding claim 12, a selector, having multiple channels, logic for selecting a subset of said channels for further processing, and apparatus associated with each of said channels for determining the quality of a digital signal, comprising: a sampler using clock cycles for sampling the digital signal with a number n of samples per defined pulse width, whereby $n \geq 1$; an edge detector for detecting an edge of a pulse of the sampled digital signal; a counter for counting the clock cycles between edges detected by the edge detector; and a deviation detector being able to compare the counted clock cycle with a prestored reference value in order to provide a deviation value as a measure for the instantaneous quality of the digital signal; **wherein the logic comprises a minimum detector for detecting a digital signal with the best signal quality measure and a primary multiplexer for selecting the digital signal for further processing.**

c. Regarding claim 14, a selector, having multiple channels, logic for selecting a subset of said channels for further processing, and apparatus associated with each of said channels for determining the quality of a digital signal, comprising: a sampler using clock cycles for sampling the digital signal with a number n of samples per defined pulse width, whereby $n \geq 1$; an edge detector for detecting an edge of a pulse of the sampled digital signal; a counter for counting the clock cycles between edges detected by the edge detector; and a deviation detector being able to compare the counted clock cycle with a prestored reference value in

order to provide a deviation value as a measure for the instantaneous quality of the digital signal; wherein the logic comprises a minimum-maximum detector for detecting a first digital signal with the best signal quality measure and a second digital signal with the second-best quality measure and a diversity multiplexer for selecting these digital signals for further processing.

d. Regarding claim 16, there is no prior art that teaches a receiver system including a channel multiplexer having logic including a minimum-maximum detector for detecting a first digital signal with best signal quality measure and a second digital signal with second-best quality measure and a diversity multiplexer for selecting these digital signals for further processing and **a channel detector for determining a pulse position that bases on the first digital signal with the best signal quality measure and the second digital signal with the second-best signal quality measure, the apparatus comprising: a first storage unit for storing at least one symbol of the first digital signal with the best signal quality measure; a second storage unit for storing at least one symbol of the second digital signal with the second-best signal quality measure; and a determination unit comprising a probability table, which in case that the first and second digital signals are received is addressed with the at least one symbol of the first digital signal with the best signal quality measure and the at least one symbol of the second digital signal with the second-best signal quality measure, thereby providing a value that is defined as the pulse position.**

e. Regarding claim 17, a method for determining the quality of a digital signal comprising: sampling the digital signal with a number n of samples per defined pulse width, where $n \geq 1$: detecting an edge of a pulse of the sampled digital signal; counting the clock cycles between edges; comparing the counted clock cycles with a prestored reference-value in order to output a deviation value as a measure for the instantaneous quality of the digital signal; and **feeding the deviation value to an absolute-value limiter unit that provides an absolute deviation value and feeding the absolute deviation value to a storage latch that outputs the absolute deviation value for further processing.**

f. Regarding claim 25, there is no prior art that teaches a method for determining quality of a digital signal comprising sampling the digital signal with a number n of samples per defined pulse width, whereby $n \geq 1$; detecting an edge of a pulse of the sampled digital signal; counting the clock cycles between edges; and comparing the counted clock cycles with a pre-stored reference value in order to output a deviation value as a measure for the instantaneous quality of the digital signal; and **further comprising the following steps for determining a pulse position for the digital signal, which is received as at least a first digital signal and a second digital signal: storing a probability table; storing at least one symbol of the first digital signal; storing at least one symbol of the second digital signal; and addressing the probability table with the at least one symbol of the first digital signal and the at least one symbol of the second digital signal, thereby the probability table providing a value that is defined as the pulse position.**

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Krista M. Flanagan whose telephone number is (571) 272-2203. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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